

RECEIVED  
CENTRAL FAX CENTER  
DEC 17 2007

PATENT  
Docket No: CX03022USU (04CXT0006D)  
Serial No.: 10/751,013

AMENDMENTS

TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A DC offset correction system for a direct-conversion receiver that includes a baseband section that has an input and an output, the DC offset correction system comprising:

a DC feedback correction servo-loop in signal communication with the baseband section, wherein the DC feedback correction servo-loop is coupled to both the input and output of the baseband section; and

an attenuator within the DC feedback correction servo-loop capable of generating an attenuation coefficient  $k_{fb}$ .

2. (original) The DC offset correction system of claim 1, wherein the DC feedback correction servo-loop includes:

an integrator circuit in signal communication with the output of the baseband section; and  
a combiner circuit in signal communication with the input of the baseband section.

3. (canceled)

PATENT

Docket No: CX03022USU (04CXT0006D)

Serial No.: 10/751,013

4. (previously presented) The DC offset correction system of claim 2, wherein the attenuator includes a resistor and a Sallen-Key RC filter.

5. (original) The DC offset correction system of claim 2, wherein the integrator circuit is a RC filter.

6. (original) The DC offset correction system of claim 2, wherein the integrator circuit is a non-RC filter.

7. (canceled)

8. (currently amended) The DC offset correction system of claim [[7]]1, wherein the attenuator includes a resistor and a Sallen-Key RC filter.

9. (original) The DC offset correction system of claim 8, further including a controller in signal communication with the baseband section and the attenuator.

10. (previously presented) The DC offset correction system of claim 2, further including a controller in signal communication with the baseband section and the attenuator.

11. (original) The DC offset correction system of claim 1, further including a controller in signal communication with the baseband section and the attenuator.

PATENT

Docket No: CX03022USU (04CXT0006D)

Serial No.: 10/751,013

12. (original) A DC offset correction system for a direct-conversion receiver that includes a baseband section that has an input and an output, the DC offset correction system comprising:

a DC feedback correction servo-loop in signal communication with the baseband section, wherein the DC feedback correction servo-loop is coupled to both the input and output of the baseband section; and

means for producing an attenuation coefficient  $k_{fb}$  within the DC feedback correction servo-loop, the attenuation means in signal communication with the input of the baseband section.

13. (original) The DC offset correction system of claim 12, wherein the DC feedback correction servo-loop includes:

a means for integrating a received signal from the output of the baseband section; and

a means for combining an attenuated feedback signal produced by the attenuation means with received signals to the input of the baseband section.

14. (canceled)

15. (previously presented) The DC offset correction system of claim 13, wherein the attenuator means includes a resistor and a Sallen-Key RC filter.

PATENT  
Docket No: CX03022USU (04CXT0006D)  
Serial No.: 10/751,013

16. (previously presented) The DC offset correction system of claim 13, wherein the means for integrating includes a RC filter.

17. (previously presented) The DC offset correction system of claim 13, wherein the means for integrating includes a non-RC filter.

18. (previously presented) A method for correcting for DC offset in a direct-conversion receiver that includes a baseband section that has an input and an output utilizing a DC offset correction system, the method comprising:

processing a received baseband output signal from the output of the baseband section to create a processed feedback signal;

attenuating the processed feedback signal with an attenuation coefficient  $k_f$  to create an attenuated feedback signal;

transmitting the attenuated feedback signal to the input of the baseband section.

19. (previously presented) The method of claim 18, wherein processing includes integrating the received baseband output signal with an integrator circuit.

20. (previously presented) The method of claim 18, wherein attenuating includes generating the attenuation coefficient  $k_f$  utilizing a resistor for a summation with a Sallen-Key RC filter.

PATENT  
Docket No: CX03022USU (04CXT0006D)  
Serial No.: 10/751,013

21. (previously presented) The method of claim 20, wherein the attenuation coefficient  $k_{fb}$  is implemented by the ratio of a feedback resistor over the resistor in the input path as Sallen-Key RC filter.

22. (previously presented) The method of claim 18, wherein transmitting includes combining the attenuated feedback signal with an input signal that is being input into the baseband section.

23. (previously presented) The DC offset correction system of claim 10, wherein the controller generates a control signal that adjusts the attenuation coefficient  $k_{fb}$ .

24. (previously presented) The DC offset correction system of claim 10, wherein the controller generates a control signal that enables the attenuation coefficient  $k_{fb}$  to track the gain of the baseband section.

25. (previously presented) The DC offset correction system of claim 2, wherein the DC feedback correction servo-loop is arranged to operate according to a high-pass transfer function as follows:

$$\frac{V_o}{V_i} = A_{ff} \frac{s}{s + \frac{A_{ff} k_{fb}}{RC}},$$

PATENT

Docket No: CX03022USU (04CXT0006D)

Serial No.: 10/751,013

where  $V_i$  is an input voltage into the system,  $V_o$  is an output voltage of the baseband section,  $s$  is a Laplace transform operator,  $A_f$  is the forward gain of the baseband section,  $R$  is a resistance of the integrator circuit, and  $C$  is a capacitance of the integrator circuit.

26. (previously presented) The DC offset correction system of claim 13, further including a controller in signal communication with the baseband section and the attenuator means.

27. (previously presented) The DC offset correction system of claim 26, wherein the controller generates a control signal that adjusts the attenuation coefficient  $k_b$ .

28. (previously presented) The DC offset correction system of claim 26, wherein the controller generates a control signal that enables the attenuation coefficient  $k_b$  to track the gain of the baseband section.

29. (previously presented) The DC offset correction system of claim 13, wherein the DC feedback correction servo-loop is arranged to operate according to a high-pass transfer function as follows:

$$\frac{V_o}{V_i} = A_f \frac{s}{s + \frac{A_f k_b}{RC}},$$

PATENT

Docket No: CX03022USU (04CXT0006D)

Serial No.: 10/751,013

where  $V_i$  is an input voltage into the system,  $V_o$  is an output voltage of the baseband section,  $s$  is a Laplace transform operator,  $A_{ff}$  is the forward gain of the baseband section,  $R$  is a resistance of the integrator means, and  $C$  is a capacitance of the integrator means.

30. (previously presented) The method of claim 18, further including controlling the attenuating wherein the attenuation coefficient  $k_p$  tracks the gain of the baseband section.

31. (previously presented) The method of claim 19, wherein the feedback signal is processed in a DC feedback correction servo-loop of the DC offset correction system that is coupled to an input and an output of the baseband section, integrating includes operating an integrator circuit of the DC offset correction system, and the method further includes operating the DC feedback correction servo-loop according to a high-pass transfer function as follows:

$$\frac{V_o}{V_i} = A_{ff} \frac{s}{s + \frac{A_{ff} k_p}{RC}},$$

where  $V_i$  is an input voltage into the system,  $V_o$  is an output voltage of the baseband section,  $s$  is a Laplace transform operator,  $A_{ff}$  is the forward gain of the baseband section,  $R$  is a resistance of the integrator circuit, and  $C$  is a capacitance of the integrator circuit.